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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,963	01/22/2002	Aron T. Lunde	37829.0400	5214

20322 7590 02/02/2007

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/053,963	LUNDE, ARON T.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-10 and 12-28* is/are rejected.

7)☒ Claim(s) *3,6 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20070131* .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Applicant's Amendment and Arguments

1. The non-final rejection as set forth in paper No. (20060810) mailed on August 16th, 2006 is withdrawn in response to applicants' amendments. A new rejection is made as set forth in this Office Action. Claims (1-28) are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-5, 7-10, and 12-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Han et al. (U.S. Patent 6,429,532).

In re claim 1, **Han** discloses a method for preparing a die on a wafer for testing by a testing apparatus, the method comprising, forming a die 200 on a wafer, the die 200 having an active portion comprising integrated circuitry, wherein the die 200 has a plurality of input bond pads 212b formed on the active portion; forming a plurality of test pads 212a on the die 200 the plurality of test pads 212a accessible to the testing apparatus (probe) 210, at least one of the plurality of test pads 121a corresponding to at least one of the plurality of input bond pads 212b; forming a conductive path between the at least one of the plurality of test pads 212a and the at least one of the plurality of input bond pads 212b, wherein a portion of the conductive path is formed on the die 200 between an edge

of the die 200 and the active portion of the die 30 (col. 2, lines 33-55 and FIGS. 2-3); and testing the die 200 by contacting the at least one of plurality of test pads 212a with the testing apparatus 210 (col. 2, lines 33-54 and FIGS. 2-3).

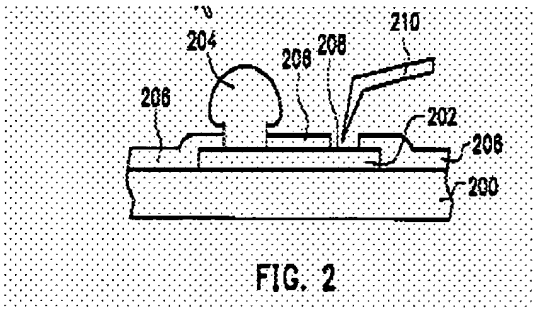

FIG. 2

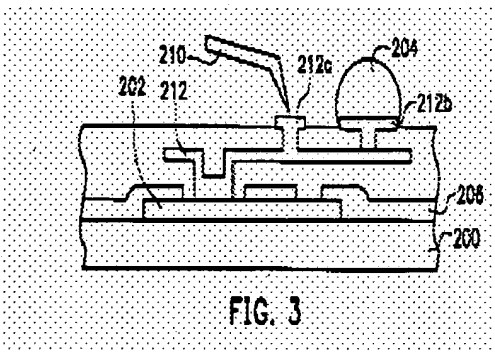

FIG. 3

In re claim 2, as applied to claim 1 above, **Han** discloses all claimed limitations including the limitation wherein the plurality of test pads 212a is formed on the active portion of the die 200 (col. 2, lines 44-55).

In re claim 4, as applied to claim 1 above, **Han** discloses all claimed limitations including the limitation wherein portion of the conductive path is formed on wafer outside of the die 200 (FIGS. 2-3).

In re claim 5, as applied to claim 1 above, **Han** discloses all claimed limitations including the limitation wherein severing the conductive path at a point outside of the active portion of the die 200 (FIG. 3).

In re claim 7, as applied to claim 4 above, **Han** discloses all claimed limitations including the limitation wherein severing the conductive path at a point outside the die 200 (FIG. 3).

In re claim 8, as applied to claim 1 above, **Han** discloses all claimed limitations including the limitation wherein at least one test pad 212a is of a sufficient size so as to be accessible by a testing apparatus 210 (probe) (col. 2, lines 34-43).

In re claim 9, **Han** discloses a die assembly formed on a wafer, the die assembly comprising, a die 200 formed on a wafer, the die 200 having an active portion comprising integrated circuitry, at least one input bond pad 212b formed on the active portion of the die 200; at least one test pad 212a formed entirely on the die 200; and a conductive path that electrically couples the at least one input bond pad 212b to the at least one test pad 212a, wherein a portion of the conductive path is formed between an edge of the die 200 and the active portion of the die 200 (col. 2, lines 33-54 and FIGS. 2-3).

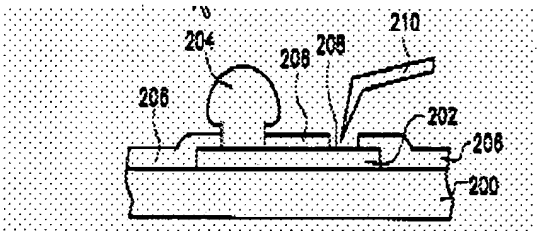

FIG. 2

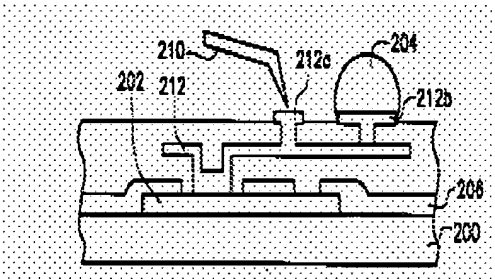

FIG. 3

In re claim 10, as applied to claim 9 above, **Han** discloses all claimed limitations including the limitation wherein the plurality of test pads 212a is formed on the active portion of the die 200 (col. 2, lines 44-55).

In re claim 12, as applied to claim 9 above, **Han** discloses all claimed limitations including the limitation wherein the die being surround by a non-conducting scribe area on the wafer, wherein the portion of the conductive path is formed on the non-conducting scribe area (FIG. 3).

In re claim 13, as applied to claim 9 above, **Han** discloses all claimed limitations including the limitation wherein at least one test pad 212a is of a sufficient size so as to be accessible by a testing apparatus 210 (probe) (col. 2, lines 34-43).

In re claim 14, **Han** discloses a method for preparing a die on a wafer for testing by a testing apparatus, the method comprising, forming a die 200 on a wafer, the die having an active portion comprising integrated circuitry, forming a plurality of input bond pads 212b on the active portion; forming a plurality of test pads 212a entirely on the die 200, wherein the plurality of test pads 212a accessible to the testing apparatus 210 (probe) (col. 2, lines 34-43), at least one of the plurality of test pads 212a corresponding to at least one of the plurality of input bond pads 212b; forming a conductive path between the at least one of the plurality of test pads 212a and the at least one of the plurality of input bond pads 212b, wherein a portion of the conductive path is formed on the die between an edge of the die 200 and the active portion of the die 200 (col. 2, lines 33-54 and FIGS. 2-3); and testing the die 200 by contacting the at least one of plurality of test pads 212a with the testing apparatus 210 (probe) (col. 2, lines 44-55).

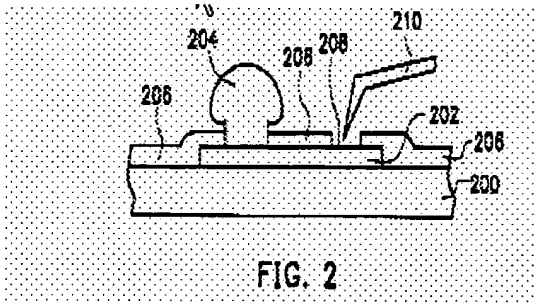

FIG. 2

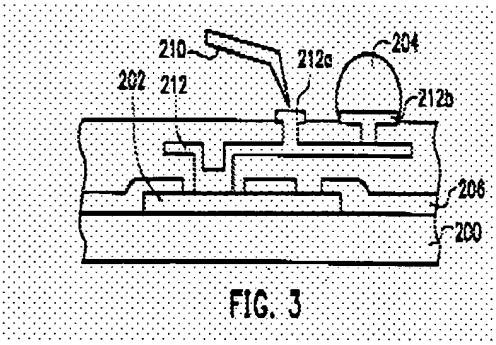

FIG. 3

In re claim 15, as applied to claim 14 above, **Han** discloses all claimed limitations including the limitation wherein the plurality of test pads 212a is formed on the active portion of the die 200 (col. 2, lines 44-55).

In re claim 16, as applied to claim 14 above, **Han** discloses all claimed limitations including the limitation wherein the active portion being surrounded by an inactive portion, wherein the portion of the conductive path is formed on the inactive portion (FIG. 3).

In re claim 17, as applied to claim 14 above, **Han** discloses all claimed limitations including the limitation wherein portion of the conductive path is formed on wafer outside of the die 200 (FIG. 3).

In re claim 18, as applied to claim 14 above, **Han** discloses all claimed limitations including the limitation wherein severing the conductive path at a point outside of the active portion of the die 200 (FIG. 3).

In re claim 19, as applied to claim 16 above, **Han** discloses all claimed limitations including the limitation wherein severing the conductive path at a point within the inactive portion (FIG. 3).

In re claim 20, as applied to claim 17 above, **Han** discloses all claimed limitations including the limitation wherein severing the conductive path at a point outside the die 200 (FIG. 3).

In re claim 21, as applied to claim 14 above, **Han** discloses all claimed limitations including the limitation wherein at least one of the plurality of test pad 212a is larger in size than the at least one of the plurality of the input bond pads 212b (col. 2, lines 52-55).

In re claim 22, **Han** discloses a die comprising, an active portion comprising integrated circuitry; a plurality of input bond pads 212b formed on the active portion; a plurality of test pads 212a formed entirely on the die 200, and the plurality of conductive lines, wherein each of the conductive lines is initially formed to electrically couple at least one of the plurality of input bond pads 212b to at least one of the plurality of test pads 212a, and wherein a portion of each of the conductive lines is formed on an area between an edge of the die 200 and the active portion of the die 200 (col. 2, lines 33-54 and FIGS. 2-3).

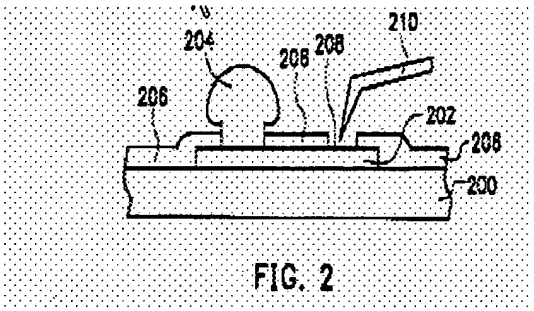

FIG. 2

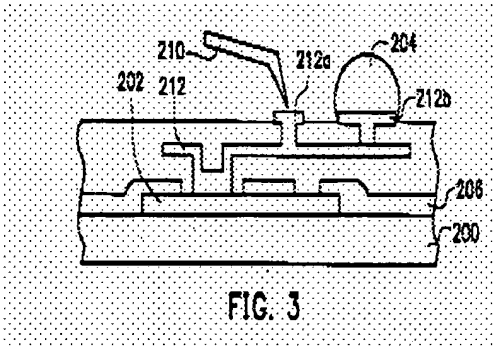

FIG. 3

In re claim 23, as applied to claim 22 above, **Han** discloses all claimed limitations including the limitation wherein the plurality of test pads 212a is formed on the active portion of the die 200 (FIG. 3).

In re claim 24, as applied to claim 22 above, **Han** discloses all claimed limitations including the limitation wherein the active portion being surrounded by an inactive portion, wherein the portion of each of the conductive lines is formed on the inactive portion and is subsequently severed at a point on the inactive portion (FIG. 3).

In re claim 25, as applied to claim 22 above, **Han** discloses all claimed limitations including the limitation wherein portion of the conductive lines is formed on wafer outside of the die 200 and is subsequently severed at a point outside the die (FIG. 3).

In re claim 26, as applied to claim 25 above, **Han** discloses all claimed limitations including the limitation wherein the portion of each of the conductive lines is severed when the die 200 is separated from the wafer (FIG. 3).

In re claim 27, as applied to claim 22 above, **Han** discloses all claimed limitations including the limitation wherein the at least one of the plurality of test pads is larger in size than the at least one of the plurality of input bond pads (col. 2, lines 52-55).

In re claim 28, **Han** discloses a die comprising, an active portion comprising integrated circuitry, a plurality of input bond pads 212a formed on the active portion; a plurality of test pads 212a formed on the die 200, a plurality of conductive lines, wherein each of the conductive lines is initially formed to electrically couple the at least one of the plurality of input bond pad 212b to the at least one of the plurality of test pad 212a, and wherein a portion of each of the conductive lines is formed on a scribe area outside the die 200 (col. 2, lines 33-54 and FIGS. 2-3).

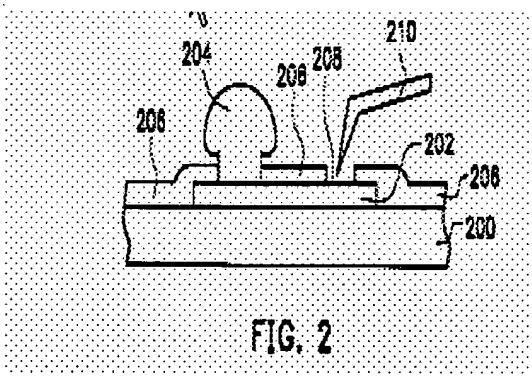

FIG. 2

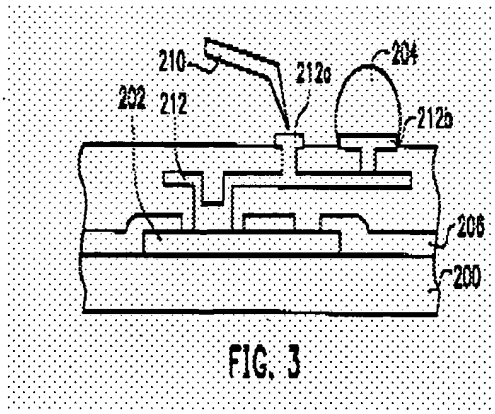

FIG. 3

Allowable Subject Matter

4. Claims 3, 6, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Applicant's Amendment and Arguments

5. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
January 31, 2007

Brook Kebede
BROOK KEBEDE
PRIMARY EXAMINER